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Description

HIGH-TO-LOW LEVEL SHIFTER

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a level shifter, and more particularly, to a level shifter for shifting the voltage level of a logic signal from a high operating voltage to a low operating voltage.

[0003] 2. Description of the Prior Art

[0004] In an integrated circuit, because of the concerns of power and integration, the operating voltage of the integrated circuit is usually smaller than the operating voltage of an external system. Take an integrated circuit using 1.2V as the operating voltage as an example, 1.2V and 0V are used to represent logic value 1 and 0 respectively. But an external circuit usually uses higher voltage as the operating voltage than the integrated circuit. For example, the operating voltage of circuit elements on a motherboard is normally 5V or 3.3V, that is, 5V or 3.3V is used to repre-

sent logic value 1, while 0V is used to represent logic value 0. Accordingly, in an integrated circuit, a device must be set for shifting the level of a logic signal switching between 5V(or 3.3V) and 0V into a logic signal switching between 1.2V and 0V, which is termed "high-to-low level shifter" hereinafter.

[0005] In an integrated circuit, a component operating at 5V/3.3V is conventionally called high-voltage element; a component operating at 1.2V is conventionally called low-voltage element. Take a metal-oxide-semiconductor transistor (MOS transistor) as an example, being a high-voltage element or a low-voltage element is determined by the thickness of the oxide-layer of the MOS transistor. Generally speaking, a high-voltage MOS transistor has thicker oxide-layer than a low-voltage MOS transistor. Consequently, the threshold voltage of the high-voltage MOS transistor is larger than the threshold voltage of the low-voltage MOS transistor. Normally a high-voltage MOS transistor has a nominal threshold voltage of 0.9V.

[0006] Please refer to Fig.1, a circuit diagram of a conventional high-to-low level shifter is illustrated. In Fig.1 a high-to-low level shifter 100 is set inside an integrated circuit 150, and is coupled to an external circuit 180. The oper-

ating voltages of the external circuit 180 are: VDDH=3.3V, VSSH=0V, and the operating voltages of the integrated circuit 150 are: VDDL=1.2V, VSSL=0V. The high-to-low level shifter 100 includes: a high-voltage PMOS transistor 140 and a high-voltage NMOS transistor 160. Because the level shifter 100 receives the logic signal from the external circuit 180, the elements of the level shifter 100 are preferably high-voltage elements. When an external signal SH1 is at logic 1, its potential equals VDDH, the high-voltage NMOS transistor 160 will be turned on, and as a result the potential of an internal signal SL1 will be pulled down to VSSL. On the contrary, when the external signal SH1 is at logic 0, its potential equals VSSH, the high-voltage PMOS transistor 140 will be turned on, and as a result the potential of the internal signal SL1 will be pulled up to VDDL.

[0007] Please refer to Fig.2, an example of logic signals in Fig.1 is illustrated. From Fig.2 it can be seen that under circumstances described above, logic signals can pass through the high-to-low level shifter 100 correctly.

[0008] But with advanced technology on integrated circuit processes, the operating voltage of the integrated circuit becomes smaller and smaller. For example, an integrated

circuit produced through advanced technology can have operating voltage lower than 1.2, such as 0.9V or even lower. Under such circumstances the high-to-low level shifter 100 of Fig.1 will probably pass logic signals wrongly.

[0009] Take VDDL=1V as an example (assume other parameters are unchanged). When the potential of the external signal SH1 equals VDDH, the potential of the internal signal SL1 will be pulled down to VSSL by the high-voltage NMOS transistor 160. However, when the potential of the external signal SH1 equals VSSH, even though the channel between the drain and the source of the high-voltage PMOS transistor 140 is turned on, the equivalent resistance of the channel is not small enough to be ignored, so it takes much more time for the internal signal SL1 to raise toward VDDL, and the switching time for the integrated circuit 150 is then increased. Under an extreme situation, while the operating frequency of the external signal SH1 is raised, each time when the potential of the external signal SH1 equals VSSL, the time period may not be enough for the potential of the internal signal SL1 to rise to VDDL. Under such circumstances the logic signal outputted (SL1) by the level shifter 100 will be incorrect as it is shown in

Fig.3.

[0010] When VDDL equals 0.9V, or even smaller than 0.9V (assume that other parameters are unchanged), because the threshold voltage of high-voltage elements is 0.9V, when the potential of the external signal equals VSSH, the channel of the high-voltage PMOS transistor 140 will not be turned on, and accordingly the logic signals outputted (SL1) by the level shifter 100 will be incorrect as it is shown in Fig.4.

[0011] As depicted above, one difficulty the high-to-low level shifter in Fig.1 faces is that logic signal probably can not pass through the high-to-low level shifter correctly when the operating voltage of the integrated circuit becomes smaller and smaller.

SUMMARY OF INVENTION

[0012] It is therefore one of the many objectives of the claimed invention to provide a high-to-low level shifter including an inverter and a level shifter.

[0013] According to the claimed invention, a high-to-low level shifter includes: an inverter for receiving an input signal and generating an inverse input signal, wherein the inverter operates using a first voltage; and a level shifter for generating an output signal according to the input signal

and the inverse input signal, wherein the level shifter operates at a second voltage, the logic level of the output signal corresponds to the second voltage, and the logic value of the output signal corresponds to the input signal.

[0014] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the embodiments that are illustrated in the various figures and drawings.

Brief Description of Drawings

[0015] Fig.1 is a circuit diagram of a conventional high-to-low level shifter.

[0016] Fig.2 is an example of logic signals in Fig.1.

[0017] Fig.3 is an example of logic signals in Fig.1.

[0018] Fig.4 is an example of logic signals in Fig.1.

[0019] Fig.5 is a circuit diagram of a high-to-low level shifter according to an embodiment of the present invention.

[0020] Fig.6 is an example of logic signals in Fig.5.

[0021] Fig.7 is a circuit diagram of a high-to-low level shifter according to another embodiment of the present invention.

[0022] Fig.8 is an example of logic signals in Fig.7.

DETAILED DESCRIPTION

[0023] Please refer to Fig.5, a circuit diagram of a high-to-low level shifter according to a first embodiment of the present invention is illustrated. A high-to-low level shifter 500 is coupled to an external first signal SH1, for shifting the level of the external first signal SH1 to become an internal signal SL1, wherein the potential of the external first signal SH1 substantially switches between VDDH (5V/3.3V) and VSSH (0V), while the potential of the internal signal SL1 substantially switches between VDDL (smaller than 0.9V in this embodiment) and VSSL (0V). The high-to-low level shifter 500 includes: an inverter 520, for receiving the external first signal SH1 and in turn generating an external second signal SH2; a pull-up element, which in this embodiment is a high-voltage NMOS transistor 540, coupled to the inverter 520; and a pull-down element, which in this embodiment is a high-voltage NMOS transistor 560, coupled to the external first signal SH1. In this embodiment, the inverter 520 is set inside as part of an external circuit, while the pull-up element 540 and the pull-down element 560 are set inside as part of an integrated circuit, and the pull-up element 540 and the pull-down element 560 are both high-voltage elements

with threshold voltage equal to 0.9V.

[0024] When the external first signal SH1 is at logic 1, its potential substantially equals VDDH, and the inverter 520 outputs the external second signal SH2 with potential equals VSSH. Under such circumstances, the high-voltage NMOS transistor 560 will be turned on while the high-voltage NMOS transistor 540 will be turned off. Because at this time the channel of the high-voltage NMOS transistor 560 is equivalent to a small resistor, the potential of the internal signal SL1 will be pulled down to VSSL very fast.

[0025] On the contrary, when the external first signal SH1 is at logic 0, its potential substantially equals VSSH, and the inverter 520 outputs the external second signal SH2 with potential equals VDDH. Under such circumstances the high-voltage NMOS transistor 560 will be turned off while the high-voltage NMOS transistor 540 will be turned on. Because at this time the high-voltage NMOS transistor 540 is equivalent to a small resistor, the potential of the internal signal SL1 will be pulled up to VDDL very fast.

[0026] Please refer to Fig.6, an example of logic signals in Fig.5 is illustrated. From Fig.6 it can be seen that, under circumstances described above, logic signals can pass through the high-to-low level shifter 500 correctly.

[0027] Please refer to Fig.7, a second embodiment circuit diagram of a high-to-low level shifter of the present invention is illustrated. The difference between Fig.7 and Fig.5 is that in Fig.7 the pull-up element (that is, the high-voltage NMOS transistor 740) coupled to the external first signal SH1, and the pull-down element (that is, the high-voltage NMOS transistor 760) coupled to the external second signal SH2 outputted by the inverter 720. The operating principle of the circuit of Fig.7 is essentially similar to that of the circuit of Fig.5, and as a result logic signals can pass through the high-to-low level shifter 700 even when VDDL is smaller than 0.9V. Please note that in Fig.5 the phase of the external first signal SH1 is inverse to the internal signal SL1, while in Fig.7 the external first signal SH1 has the same phase as the internal signal SL1. Fig.8 is an example of logic signals of Fig.7.

[0028] The high-to-low level shifter according to embodiments of the present invention can pass logical signals correctly even thought the operating voltage of the integrated circuit becomes smaller and smaller. In other words, logic signal in the external circuit with high operating voltage can be shifted to logic signals in the integrated circuit with low operating voltage correctly.

[0029] Those skilled in the art will readily observe that numerous modification and alternation of the device may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.